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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/808,393	03/25/2004	Noriko Sasada	500.43702X00	5544

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ANTONELLI, TERRY, STOUT & KRAUS, LLP
1300 NORTH SEVENTEENTH STREET
SUITE 1800
ARLINGTON, VA 22209-3873

EXAMINER	
DICKEY, THOMAS L	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 07/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/808,393	SASADA ET AL.	
	Examiner	Art Unit	
	Thomas L. Dickey	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,17-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 17-32* is/are rejected.

7)☒ Claim(s) *3-6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed on 07/11/05 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

A. Claims 1,17,19-23,25, 27-29,31, and 32 are rejected under 35 U.S.C. 102(b) as being anticipated by Nei (2002/0158257).

With regard to claim 1 Nei discloses a chip carrier including a dielectric or semiconductor substrate 1, one surface of which includes a first metal-coated portion (part of electrode 2 opposite side 2a) and a opposite surface of which includes a second metal-coated mount portion 2a to at least one high-frequency device 4, wherein said first metal-coated portion of said one surface of substrate 1 is connected with said second metal-coated mount portion 2a of said opposite surface through a third metal-

coated portion (note that electrode 2 covers the top, bottom, and all exposed sides of substrate 1) formed on a side surface of the substrate 1. Note figures 1 and 2A-C and paragraphs 22-25 of Nei.

With regard to claim 17 Nei discloses a chip carrier including a dielectric or semiconductor substrate 1 having a first metal-coated portion 2a formed on a front surface of the substrate 1 to mount a device 4, and a second metal-coated portion (part of electrode 2 opposite side 2a) formed on a rear surface of the substrate 1, wherein a third metal-coated portion is formed on a side surface of the substrate 1, and wherein the first metal-coated portion 2a on the front surface of substrate 1 is connected with the second metal-coated portion (part of electrode 2 opposite side 2a) on the rear surface by the third metal-coated portion formed on the side surface of the substrate 1. Note figures 1 and 2A-C and paragraphs 22-25 of Nei.

With regard to claims 19,21, and 22 Nei discloses a chip carrier including a dielectric or semiconductor substrate 1 having a first metal-coated portion 2a formed on a front surface of the substrate 1 to mount an optical device 4, and a second metal-coated portion (part of electrode 2 opposite side 2a) formed on a rear surface of the substrate 1, wherein a third metal-coated portion is formed on a side surface of the substrate 1 closest to a position (note that electrode 2 covers 100% of the top, bottom, and all exposed sides of substrate 1, so must be closest, farthest, and all points between) at which the optical semiconductor device 4 is mounted, wherein an area of the third metal-coated portion formed on the side surface of the substrate 1 is equal to or greater (note that electrode 2 covers 100% of the top, bottom, and all exposed sides of substrate 1,which is more than 1/3) than 1/3 of the side surface, and wherein the first metal-coated portion 2a on the front surface of substrate 1 is connected with the second

metal-coated portion (part of electrode 2 opposite side 2a) on the rear surface by the third metal-coated portion formed on the side surface of the substrate 1. Note figures 1 and 2A-C and paragraphs 22-25 of Nei.

With regard to claim 23 Nei discloses a chip carrier including a dielectric or semiconductor substrate 1 having a first metal-coated portion 2a formed on a front surface of the substrate 1 to mount a device 4, and a second metal-coated portion (part of electrode 2 opposite side 2a) formed on a rear surface of the substrate 1, and an inductance reducer structure in a form of a third metal-coated portion is formed on a side surface of the substrate 1, and wherein the first metal-coated portion 2a on the front surface of substrate 1 is connected with the second metal-coated portion (part of electrode 2 opposite side 2a) on the rear surface by the third metal-coated portion formed on the side surface of the substrate 1. Note figures 1 and 2A-C and paragraphs 22-25 of Nei.

With regard to claims 25,27, and 28 Nei discloses a chip carrier including a dielectric or semiconductor substrate 1 having a first metal-coated portion 2a formed on a front surface of the substrate 1 to mount an optical semiconductor device 4, and a second metal-coated portion (part of electrode 2 opposite side 2a) formed on a rear surface of the substrate 1, and an inductance reducer structure in a form of a third metal-coated portion is formed on a side surface of the substrate 1 closest to a position (note that electrode 2 covers 100% of the top, bottom, and all exposed sides of substrate 1, so must be closest, farthest, and all points between) at which the optical semiconductor device 4 is mounted, wherein an area of the third metal-coated portion formed on the side surface of the substrate 1 is equal to or greater (note that electrode 2 covers 100% of the top, bottom, and all exposed sides of substrate 1,which is more than 1/3) than 1/3

of the side surface, and wherein the first metal-coated portion 2a on the front surface of substrate 1 is connected with the second metal-coated portion (part of electrode 2 opposite side 2a) on the rear surface by the third metal-coated portion formed on the side surface of the substrate 1. Note figures 1 and 2A-C and paragraphs 22-25 of Nei.

With regard to claims 29,31, and 32 Nei discloses an optical module comprising a chip carrier including a dielectric or semiconductor substrate 1 having a first metal-coated portion 2a formed on a front surface of the substrate 1 to mount an optical semiconductor device 4, and a second metal-coated portion (part of electrode 2 opposite side 2a) formed on a rear surface of the substrate 1 wherein a third metal-coated portion is formed on a side surface of the substrate 1 closest to a position (note that electrode 2 covers 100% of the top, bottom, and all exposed sides of substrate 1, so must be closest, farthest, and all points between) at which the optical semiconductor device 4 is mounted, wherein an area of the third metal-coated portion formed on the side surface of the substrate 1 is equal to or greater (note that electrode 2 covers 100% of the top, bottom, and all exposed sides of substrate 1,which is more than 1/3) than 1/3 of the side surface, and wherein the first metal-coated portion 2a on the front surface of substrate 1 is connected with the second metal-coated portion (part of electrode 2 opposite side 2a) on the rear surface by the third metal-coated portion formed on the side surface of the substrate 1; and the optical semiconductor device 4 mounted to the first metal-coated portion 2a on the front surface of the substrate 1. Note figures 1 and 2A-C and paragraphs 22-25 of Nei.

B. Claims 1,2,17-20,23-26,29, and 30 are rejected under 35 U.S.C. 102(e) as being anticipated by Brunner et al. (6,645,783).

With regard to claims 1 and 2 Brunner et al. discloses a chip carrier 4 including a dielectric or semiconductor substrate 14, one surface of which includes a first metal-coated portion 7 and a opposite surface of which includes a second metal-coated mount portion 5 to at least one high-frequency device 1, wherein said first metal-coated portion 7 of said one surface of substrate 14 is connected with said second metal-coated mount portion 5 of said opposite surface through a third metal-coated portion 8 formed on a side surface of the substrate 14, wherein the metal-coated portion on the front surface of the substrate 14 is connected with the metal-coated portion on the rear surface by a metallic via-hole 13 (note that part 13 is copper) formed through the substrate 14. Note figures 1 and 2, column 4 lines 60-67, and column 5 lines 1-14 and 63-64 of Brunner et al.

With regard to claims 17 and 18 Brunner et al. discloses a chip carrier 4 including a dielectric or semiconductor substrate 14 having a first metal-coated portion 5 formed on a front surface of the substrate 14 to mount a device 1, and a second metal-coated portion formed on a rear surface of the substrate 14, wherein a third metal-coated portion 8 is formed on a side surface of the substrate 14, and wherein the first metal-coated portion 5 on the front surface of substrate 14 is connected with the second metal-coated portion on the rear surface by the third metal-coated portion 8 formed on the side surface of the substrate 14, wherein the metal-coated portion on the front surface of the substrate 14 is connected with the metal-coated portion on the rear surface by a metallic via-hole 13 (note that part 13 is copper) formed through the

substrate 14. Note figures 1 and 2, column 4 lines 60-67, and column 5 lines 1-14 and 63-64 of Brunner et al.

With regard to claims 19 and 20 Brunner et al. discloses a chip carrier 4 including a dielectric or semiconductor substrate 14 having a first metal-coated portion 5 formed on a front surface of the substrate 14 to mount an optical device 1, and a second metal-coated portion formed on a rear surface of the substrate 14, wherein a third metal-coated portion 8 is formed on a side surface of the substrate 14, and wherein the first metal-coated portion 5 on the front surface of substrate 14 is connected with the second metal-coated portion on the rear surface by the third metal-coated portion 8 formed on the side surface of the substrate 14, wherein the metal-coated portion on the front surface of the substrate 14 is connected with the metal-coated portion on the rear surface by a metallic via-hole 13 (note that part 13 is copper) formed through the substrate 14. Note figures 1 and 2, column 4 lines 60-67, and column 5 lines 1-14 and 63-64 of Brunner et al.

With regard to claims 23 and 24 Brunner et al. discloses a chip carrier 4 including a dielectric or semiconductor substrate 14 having a first metal-coated portion 5 formed on a front surface of the substrate 14 to mount a device 1, and a second metal-coated portion formed on a rear surface of the substrate 14, and an inductance reducer structure in a form of a third metal-coated portion 8 is formed on a side surface of the substrate 14, and wherein the first metal-coated portion 5 on the front surface of substrate 14 is connected with the second metal-coated portion on the rear surface by

the third metal-coated portion 8 formed on the side surface of the substrate 14, including a secondary inductance reducer structure in a form of a metallic via-hole 13 (note that part 13 is copper) formed through the substrate 14 .wherein the first metal-coated portion 5 on the front surface of the substrate 14 is connected with the second metal-coated portion on the rear surface by the metallic via-hole 13 formed through the substrate 14. Note figures 1 and 2, column 4 lines 60-67, and column 5 lines 1-14 and 63-64 of Brunner et al.

With regard to claims 25 and 26 Brunner et al. discloses a chip carrier 4 including a dielectric or semiconductor substrate 14 having a first metal-coated portion 5 formed on a front surface of the substrate 14 to mount an optical semiconductor device 1, and a second metal-coated portion formed on a rear surface of the substrate 14, and an inductance reducer structure in a form of a third metal-coated portion 8 is formed on a side surface of the substrate 14, and wherein the first metal-coated portion 5 on the front surface of substrate 14 is connected with the second metal-coated portion on the rear surface by the third metal-coated portion 8 formed on the side surface of the substrate 14, wherein the first metal-coated portion 5 on the front surface of the substrate 14 is connected with the second metal-coated portion on the rear surface by a metallic via-hole 13 (note that part 13 is copper) formed through the substrate 14. Note figures 1 and 2, column 4 lines 60-67, and column 5 lines 1-14 and 63-64 of Brunner et al.

With regard to claims 23 and 30 Brunner et al. discloses an optical module comprising a chip carrier 4 including a dielectric or semiconductor substrate 14 having a first metal-coated portion 5 formed on a front surface of the substrate 14 to mount an optical semiconductor device 1, and a second metal-coated portion formed on a rear surface of the substrate 14 wherein a third metal-coated portion 8 is formed on a side surface of the substrate 14, and wherein the first metal-coated portion 5 on the front surface of substrate 14 is connected with the second metal-coated portion on the rear surface by the third metal-coated portion 8 formed on the side surface of the substrate 14; and the optical semiconductor device 1 mounted to the first metal-coated portion 5 on the front surface of the substrate 14, wherein the first metal-coated portion 5 on the front surface of the substrate 14 is connected with the second metal-coated portion on the rear surface by a metallic via-hole 13 (note that part 13 is copper) formed through the substrate 14. Note figures 1 and 2, column 4 lines 60-67, and column 5 lines 1-14 and 63-64 of Brunner et al.

Response to Arguments

3. Applicant's arguments with respect to claims 1 and 2 have been considered but are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

4. Claims 3-6 are allowed over the references of record because none of these references disclosed or can be combined to yield the claimed invention such as a chip carrier including a dielectric or semiconductor substrate, one surface of which includes a first metal-coated portion and a opposite surface of which includes a second metal-coated portion, a high frequency transmission line is arranged on said one surface of the substrate and a semiconductor device is mounted on said first metal-coated portion formed on said one surface of the substrate wherein said first metal-coated portion of said one surface of substrate is connected with said second metal-coated portion of said opposite surface through a third metal-coated portion formed on a side surface of the substrate, as recited in claim 3. Note that claim 3 requires both a high frequency line and a semiconductor device on the first surface of the dielectric or semiconductor substrate of the chip carrier, a combination of features not disclosed or suggested by Nei or Brunner et al.

Conclusion

5. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TLD
07/05

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800